

Figure 2: Traces of (a) input, (b) recovered clock, (c) recovered signal (Timescale right: 1.9 ns/div, left: 3.8 ns/div) and eye diagrams of (d) input and (e) recovered signal (timescale: 10 ps/div). Left column: synchronous; right column: asynchronous operation.

Mach-Zehnder Interferometer. The FFP filter acts as a low-Q passive optical resonator that extracts the line rate spectral component of the signal. The data packets are transformed into amplitude-modulated clock packets, as a result of the impulse response of the filter, and provide the control signal for MZI 1. The nonlinear gate operates as a hard limiter saturated by a CW at 1555.6 nm, to equalize the amplitude of the generated clock. This signal samples the input packets at the decision element (MZI 2), performing a logical AND between the data and their corresponding clocks. Both non-linear gates were hybridly integrated MZIs with 1.1 mm SOAs.

Results

The CDR was evaluated with variable length packet traffic, both synchronous and asynchronous. Typical results are shown in fig 2. The left column of Fig. 2 presents results obtained for synchronous packets, in this instance consisting of 116, 40 and 54 bits. The right hand column shows results for asynchronous packets, in this instance consisting of 40, 30 and 40 bits. Fig. 2(a) shows the input data packets, fig. 2(b) the acquired clock, fig. 2(c) the recovered data packets and fig. 2(d), (e) eye diagrams of input and recovered data signals. Fig. 2(b) shows that the acquired packet clock has a rise time of only 2 bits and a fall time of 15 bits. These time constants are defined by the finesse of the FFP and determine the bandwidth overhead that the CDR imposes.

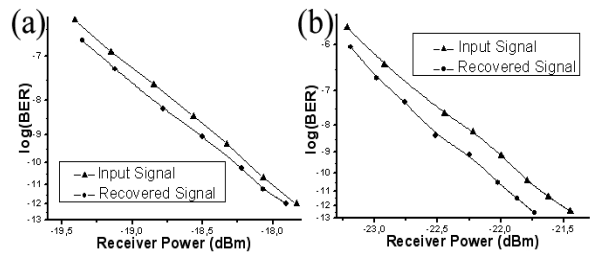


Figure 3: BER measurement for the two packet patterns in synchronous operation

The acquired eye diagrams (Fig. 2 (d)-(e)) reveal a reduction in amplitude and timing jitter owing to the regenerative properties of the circuit. Fig. 3 shows the Bit-Error-Rate performance of the circuit for the two types of packet patterns shown in Fig. 2(a), under synchronous operation. Error-free operation is achieved with negative power penalty. The timing jitter was calculated by integrating the Single Side Band (SSB) noise spectra from offset frequency of 1 kHz to 10 MHz from the carrier, providing root-mean-square (rms) values of 1.3 ps for the input, 700 fs for the clock and 870 fs for the regenerated signal. Amplitude equalization is achieved due to the nonlinear transfer function of the gate, while triggering the input data packets with the self-extracted, low-jitter clock leads to their effective retiming.

The CDR was operationally stable and compact in size, owing to the use of integrated components. The footprint for the MZIs was 72 mm×30 mm and for the FFP filter 57.2 mm×14.3mm. Integration of multiple MZIs on a single chip will decrease size and cost dramatically making a CDR circuit of the present design a realistic choice for OPS network receivers.

Conclusions

We have presented a compact, all-optical CDR circuit suitable for OPS networks. The overall bandwidth overhead is only 17 bits irrespective of packet length, providing bandwidth efficiency and fine granularity to the network. Compactness, stability and scalability offer the potential to be used in real-life applications.

Acknowledgements

The authors acknowledge support by the E.C. under project 004222 MUFINS of the FP6-IST program and Micron Optics for providing the FFP filter.

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